Testing Procedures

**Definitions**

* **Module**: Kogge-Stone and Ripple-Carry adder/comparator, 2 and 6 input MUX.
* **Top-level circuit**: the trellis optimised for speed and power

**Assumptions**

* Due to the size of the process, diffusion capacitance within each module is assumed to be much greater than wire capacitance, so will neglect.
* For presentation neglect wires in top-level circuit, but try to include for final project.

**Power Testing**

1. Generate SPICE netlist from Electric Schematic for each individual module (we are neglecting wires in power calculation of modules so no need for layout)
2. From NMOS and PMOS module definitions in SPICE, determine diffusion capacitance for each transistor in netlist.
3. For EACH module in the top-level circuit determine input/output capacitance for every input and output (ex. A[5]..A[0], B[5]..B[0], and Y[5]..Y[0]) and put in a spreadsheet. Then calculate:
   1. The average input/output diffusion capacitance for each module
   2. Maximum input/output diffusion capacitance for each module
4. Load the circuit outputs with a capacitor taking the value of the weighted average of the input capacitances.
5. Wire inputs with pulse voltage sources oscillating at the appropriate time to test all possible input combinations.
6. Run simulation to determine the power usage by probing VDD. Export data into a spreadsheet and determine average power consumption and maximum power consumption.
7. Re-perform steps 4-6 while loading circuit with maximum input capacitance.
8. Count the number of respective modules in each top-level circuit. Multiply the average and worst case module power consumption for both loading cases by the number of modules in the top-level circuit.
9. Required graphs for BOTH average and max loading:
   1. Line graphs of power usage for all input vectors vs. time – obtained from 6.
   2. Bar graphs of average and maximum power usage for each module.
   3. Bar graph of top-level circuit maximum and average power usage.

**Propagation Delay Testing**